



## Multi-core Processor Architectures

Polychronis Xekalakis and Josep M. Codina

Intel Barcelona Research Center

Aula Empressa, Facultat d'Informàtica de Barcelona, February 2010

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## Why Parallel Computing?

Simple task: Eat a pizza with 6 slices as fast as possible!!




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## Why Parallel Computing?



1x  = 6 Time Units

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## Why Parallel Computing?



1x  = 6 Time Units  
6x  = 1 Time Unit

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## Why Parallel Computing?

1x  = 6 Time Units  
6x  = 1 Time Unit

Faster ... but hungrier !!

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## Parallel Computing Promises

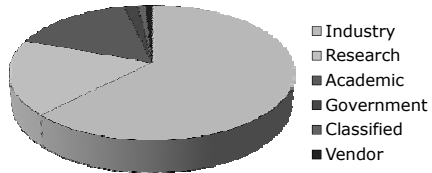
- Solve larger problems (Human genome deciphering)
- Concurrency (big datacenters)
- More economic (Google – cluster computing)
- Power efficiency (Embedded computing)

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## Who is Using Parallel Computing

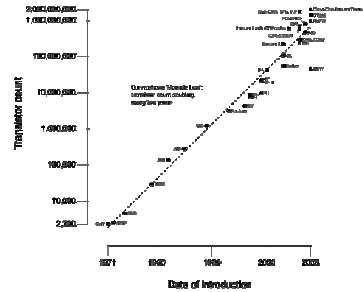


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## Moore's Law for Multi-Cores

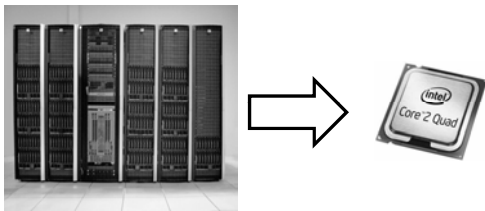
CPU Transistor Counts 1971-2008 & Moore's Law



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## Shift from Parallel Computing to Multi-cores



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## Why Chip Multiprocessors?

- For companies:
  - Time-to-market (Simply replicate cores)
  - Easier to extract perf. (Programmers have to do it ☺)
  - Power efficient (Low-cost thermal sinks)
- For individuals:
  - Solve larger problems (maybe ..)
  - Concurrency (Watch a movie, while burning a DVD)
  - Power efficiency (Embedded computing)

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## Agenda

- Motivation
- Parallel Architectures
- Keeping the Caches Consistent
- Interconnecting the cores
- Multithreading
- Concluding Remarks

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## Parallel Architectures

Data Stream	
Instruction Stream	Single Inst. Single Data SISO
	Single Inst. Multi. Data SIMD
Instruction Stream	Multi. Inst. Single Data MISD
	Multi. Inst. Multi. Data MIMD

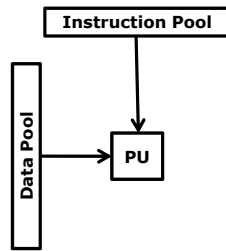
Categorization by FLYNN

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## Single Instruction Single Data

- Serial systems
- Deterministic execution
- First machines to be built
- Most common even today



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## Univac I



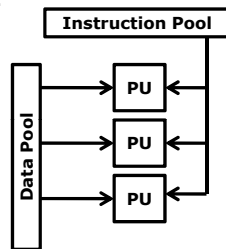
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## Single Instruction Multiple Data

- Best suited for "regular" apps.
  - graphics/image processing
- Simple SIMD units in unip.
  - MMX/SSE/ .. / AVX



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## ILLIAC IV



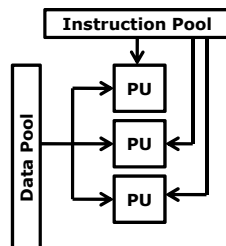
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## MISD

- Not many examples of this
- Hard to program ..



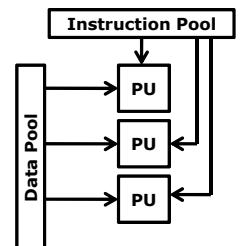
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## MIMD

- Most common supercomputer
- Everything is MIMD ..
- CMPs are MIMD too!!



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## IA32 Cluster



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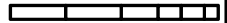
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## Caches

- Memory can be Fast or Vast !!
- Gap between Memory and Processor grows ..

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## Caches

- Memory can be Fast or Vast !!
- Gap between Memory and Processor grows ..



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## Caches

- Memory can be Fast or Vast !!
- Gap between Memory and Processor grows ..



- Caches come to the rescue ☺

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## Caches for Uniprocessors and CMPs

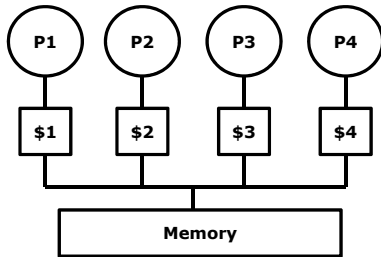
- For single core systems caches are nice:
  - Reduce average access time
  - Bigger → performance
  - Generally power efficient
- For CMPs still nice, but:
  - Cache Coherency
  - Memory Consistency

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## Cache Coherency

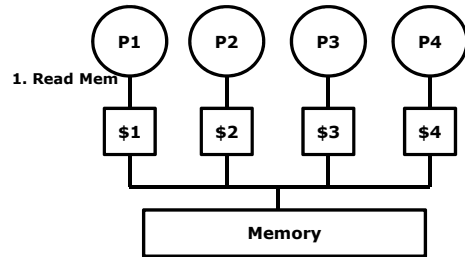


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## Cache Coherency

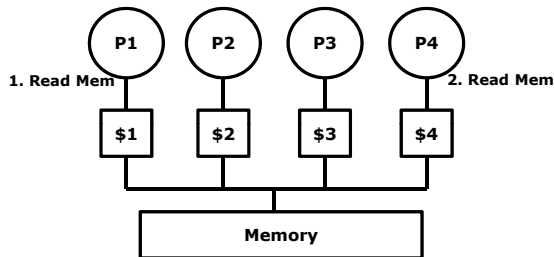


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## Cache Coherency

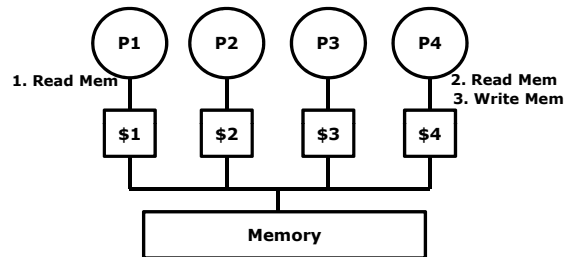


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## Cache Coherency

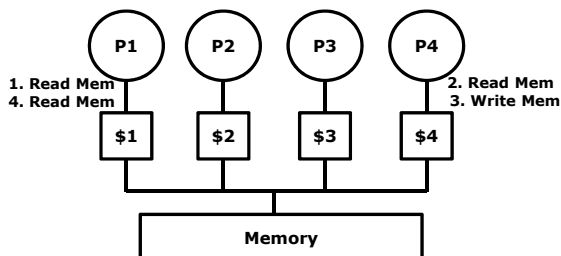


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## Cache Coherency



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## Memory Consistency

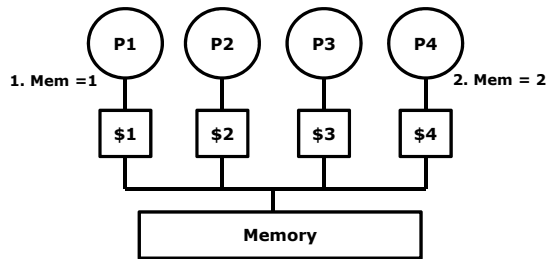
- Coherency guarantees writes visible to all
- But, in which order do they appear??

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## Memory Consistency

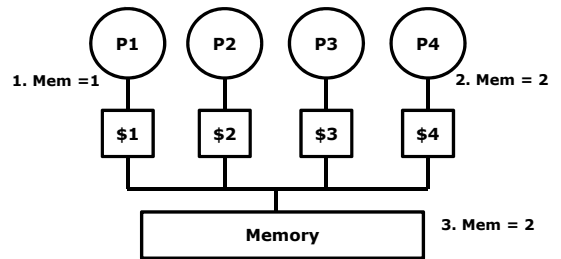


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## Memory Consistency

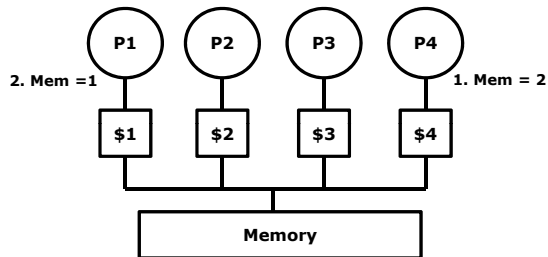


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## Memory Consistency

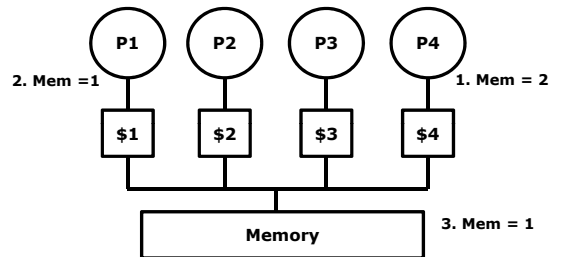


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## Memory Consistency



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## Memory Consistency Model

- Specifies constraints on the order in which memory operations (from any process) can appear to execute with respect to one another
- Implications for both programmer and system designer
  - Programmer uses to reason about correctness and possible results
  - System designer can use to constrain how much accesses can be reordered by compiler or hardware
- Contract between programmer and system

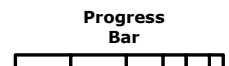
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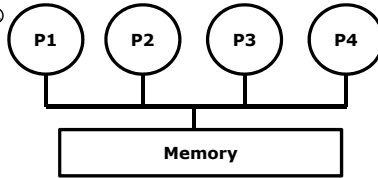
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## Simple Bus-Based Systems

- Fairly simple collection of "wires"
- Common medium that everyone can snoop
- Common for current CMPs
- Does not scale ☹



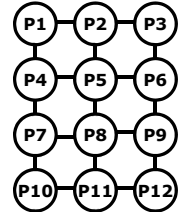
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## Mesh Networks

- Each core functions as a router
- More suitable for manycore systems
  - Single Chip Cloud Computing
- Longer latencies than bus



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## Networks on Chip

- Emerging design paradigm for interconnection within the chip
- More suitable for large-scale CMPs
  - Based on techniques used widely in networking
- NoCs provide:
  - QoS
  - Separability between computation and communication
  - Reusability

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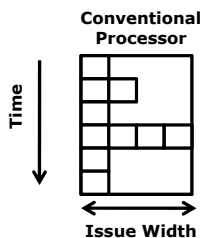
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## Multi-Threading Within a Core

- Cores usually underutilized ...



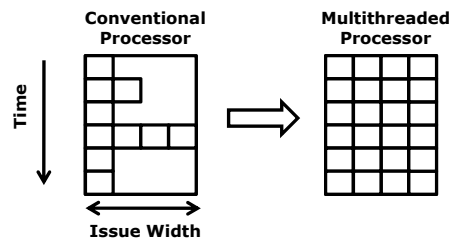
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## Simultaneous Multi-Threading

- Fill it app with instructions from other threads



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## Speculative Multithreading

- What if threads come from same app??
- Can we have threads whose sole purpose is to help the main thread??
- Yes we can (Obama)!!
  - Helper threads (prefetch to memory)
  - Multi-path (follow all paths on a branch)
  - Thread Level Speculation (extract parallelism)
  - Etc ..

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## Summary - Conclusions

- Parallel computing is here to stay
- Today we discussed about:
  - Why we need parallelism
  - What are the types of architectures
  - How we keep the memory consistent
  - Interconnections
  - Multithreading
- Tip of the iceberg: Loads of exciting research happening!!

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