System-on-Chip

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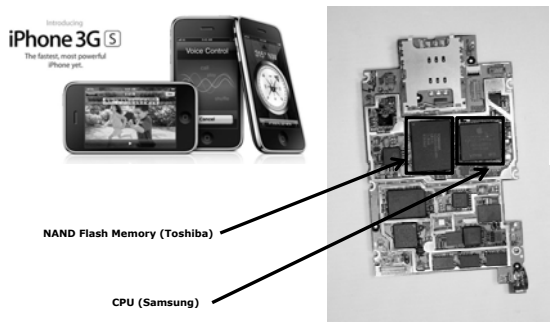
Outline

- System-on-Chip Illustrated
- SoC Challenges and Current Solutions
- Intel's Moorestown Platform
  - Designed for Next Generation Smartphones
- Future SoC:
  - Programmable Accelerator

System-on-Chip is Everywhere !

Example: iPhone 3GS disassembled



SOC contains all components required for a complete system.

SoC Challenges and Current Solutions

SoC Challenges

- Exponentially increasing SoC design complexity
- Endless Performance Requirements
- Maximum Power-efficiency

SoC Challenges – 1/3

- Exponentially increasing SoC design complexity
  - SoC = all components required for a complete system
  - 1995: < 1 million gates /one microprocessor
  - Today: 100s millions gates / multiple microprocessors
  - "*Today, as always, to be competitive, you must design almost as complex theoretically possible. If you don't, someone else will do, and the extra complexity will provide competitive edge.*"

SoC Challenges – 2/3

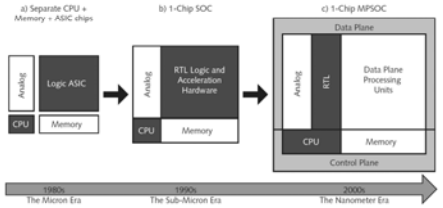
- Endless Performance Requirement
  - Multimedia: many different codec for images/audio/video
    - HD H.264 Decode: 10-50 GOPS for 30 fps (real time)
    - HD H.264 Encode: ~100 GOPS for 30 fps
    - Super Resolution: ~1000 GOPS for 30fps
  - Networking: diverse and complicated standards
    - Telephony: constant bit rate service
    - Multimedia streaming: higher bandwidth but variable bit-rate service
  - Wireless
    - Many wireless coding standard
      - Wi-Fi, WiMax, etc
    - New standards appear all the time

SoC Challenges – 3/3

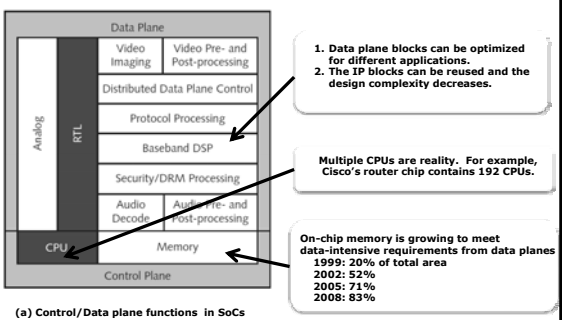
- Maximum Power-Efficiency
  - Phone: 3W power budget
    - Otherwise, the user feels too hot
  - HD.264 Decode
    - Normal PC: 45W or more, depending on the video format
    - Hardware Decoder in SoC: 100-300mW
- A big challenge
  - How to meet different performance requirements under very tight power budget?

Current SoC Design Solution: Divide and Conquer

- A SoC is divided into blocks and each block is optimized for different performance/power requirement.
  - Some blocks are control processors (control plane)
    - Programmable / flexible
  - Some blocks are data processing units and implemented with RTL hardware (data plane)



Partition of Control and Data Planes

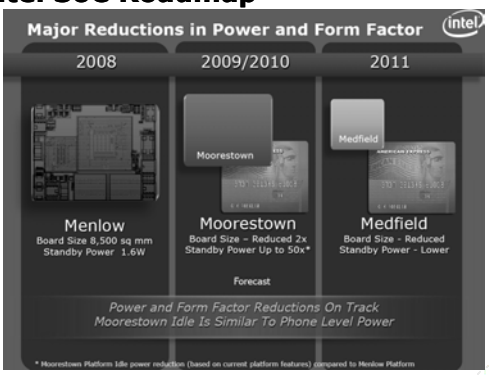


(a) Control/Data plane functions in SoCs

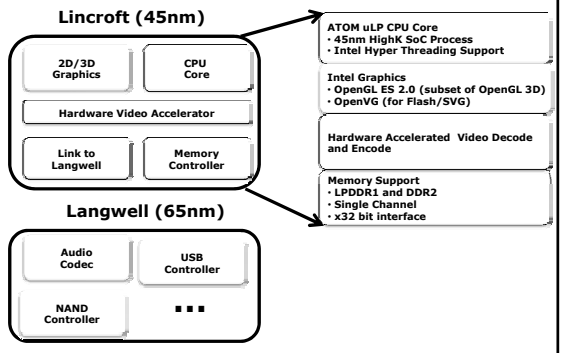
Intel's Moorestown Platform

- Designed for Next Gen Smartphones

Intel SoC Roadmap



Moorestown Platform Overview



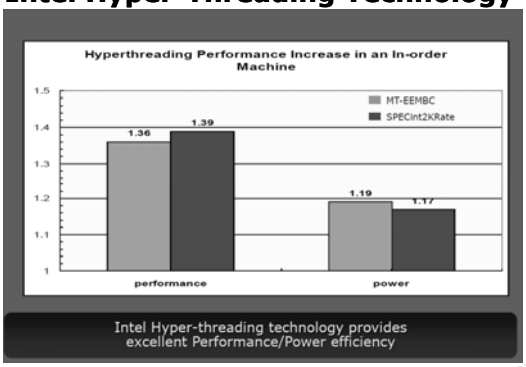
Moorestown Highlights

- High Performance for amazing Internet experience
- Dramatically lower Power
  - Up to 50x platform idle power reduction compared to Menlow Platform
- Small size for smartphone form factor

Moorestown Performance Technology

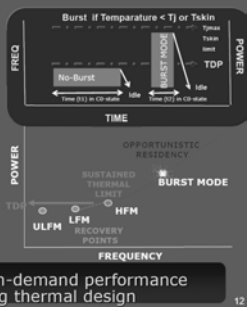
- Intel Hyper Thread Technology
- Intel Burst Performance Technology

Intel Hyper-Threading Technology



Intel Burst Performance Technology

- Taking advantage of Thermal headroom on Tj and Tskin for short duration
- On Tj and Tskin violations, System throttles to Recovery points until thermal headroom is available to burst
- Optimizes consumed energy
  - Energy(WHr)=Power x time
    - Race to idle
    - Saves energy if
      - t2/t1 < p1/p2
- Update BIOS with recommended P states for Burst Mode



Burst mode provides on-demand performance without impacting thermal design

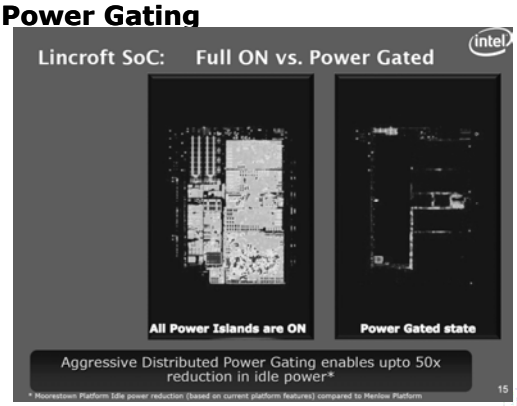
Moorestown Power Reduction

- Active Power Management – Power and Clock Gating
- Use Low Power and Handheld IO
  - LPDDR
- Accelerators (GFX, video decoder)
  - Enable functionality at low power (e.g.. HD video)

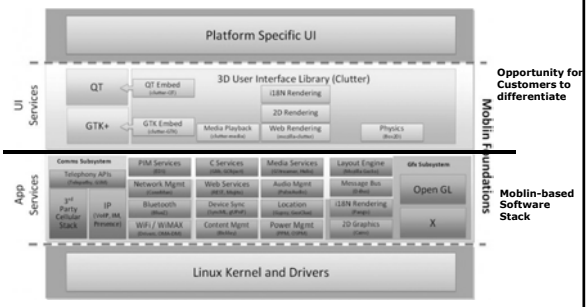
Active Power Management

- Enables long standby battery life needed for smartphones
  - Through low idle power
- Lower active scenario power by shutting things off that are not used in that mode
  - Switching off video decode block in web browsing

Power Gating



Software Development for Moorestown: Moblin

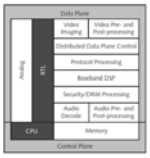


Future SoC

- Programmable Accelerator

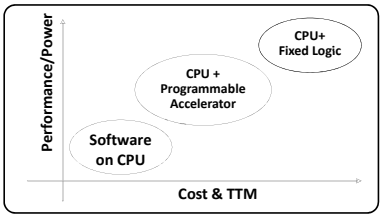
Current SoC

- IP blocks based on fixed function implementation are not programmable
  - Each data plane block cannot used for other purpose
- Long Time-to-market (TTM)
  - The block is not programmable
- High Non-Recurrent Engineering(NRE) cost

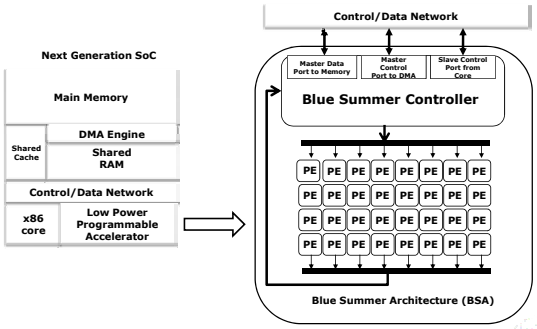


A Solution for Future SoC

- Low Power Programmable accelerator
- The challenge is to meet performance requirement under a given power and cost budget



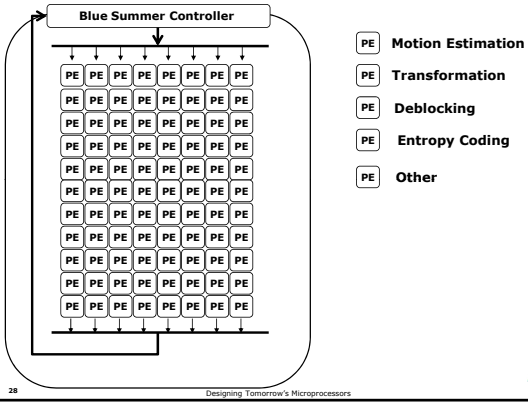
Our Programmable Accelerator: BSA



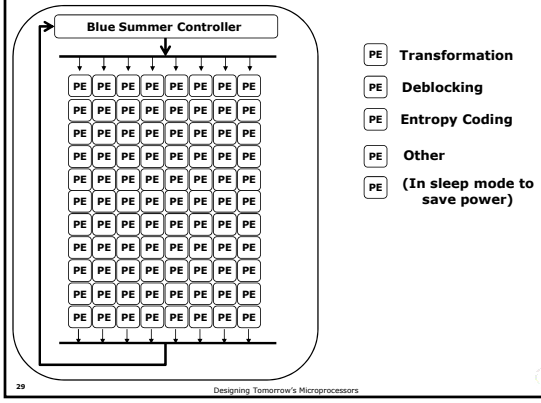
Programmable Accelerator

- Different applications can be mapped into the same programmable accelerator
- TTM & NRE cost are reduced

BSA for H264 Encoding



BSA for H264 Decoding



Take-away Messages

- SoC is everywhere!
- The SoC design challenge is to meet exponentially increasing performance requirement under tight power budget and design cost

Q & A

References

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