System-on-Chip
Qi Cong Cai
Intel Barcelona Research Center

Aula Empresa, Facultat d'Informàtica de Barcelona, February 2010

© Intel Corporation, 2010

Outline
• System-on-Chip Illustrated
• SoC Challenges and Current Solutions
• Intel’s Moorestown Platform
  – Designed for Next Generation Smartphones
• Future SoC:
  – Programmable Accelerator

System-on-Chip is Everywhere!

Example: iPhone 3GS disassembled

SoC Challenges and Current Solutions

SoC Challenges
• Exponentially increasing SoC design complexity
• Endless Performance Requirements
• Maximum Power-efficiency
SoC Challenges – 1/3

- Exponentially increasing SoC design complexity
  - SoC = all components required for a complete system
  - 1995: < 1 million gates / one microprocessor
  - Today: 100s millions gates / multiple microprocessors
- "Today, as always, to be competitive, you must design almost as complex theoretically possible. If you don’t, someone else will do, and the extra complexity will provide competitive edge."

SoC Challenges – 2/3

- Endless Performance Requirement
  - Multimedia: many different codec for images/audio/video
    - HD H.264 Decode: ~100 GOPS for 30 fps
    - HD H.264 Encode: ~120 GOPS for 30 fps
    - Super Resolution: ~1000 GOPS for 30 fps
  - Networking: diverse and complicated standards
    - Telephony: constant bit rate service
    - Multimedia streaming: higher bandwidth but variable bit-rate service
  - Wireless
    - Many wireless coding standard
      - Wi-Fi, WiMax, etc
    - New standards appear all the time

SoC Challenges – 3/3

- Maximum Power-Efficiency
  - Phone: 3W power budget
    - Otherwise, the user feels too hot
  - HD.264 Decode
    - Normal PC: 45W or more, depending on the video format
    - Hardware Decoder in SoC: 100-300mW
- A big challenge
  - How to meet different performance requirements under very tight power budget?

Current SoC Design Solution: Divide and Conquer

- A SoC is divided into blocks and each block is optimized for different performance/power requirement.
  - Some blocks are control processors (control plane)
    - Programmable / Flexible
  - Some blocks are data processing units and implemented with RTL hardware (data plane)

Partition of Control and Data Planes

1. Data plane blocks can be optimized for different applications.
2. The IP blocks can be reused and the design complexity decreases.

Intel’s Moorestown Platform

- Designed for Next Gen Smartphones

- On-chip memory is growing to meet data-intensive requirements from data planes:
  - 1999: 20% of total area
  - 2002: 52%
  - 2005: 71%
  - 2008: 83%
**Moorestown Highlights**

- **High Performance** for amazing Internet experience
- **Dramatically lower Power**
  - Up to 50x platform idle power reduction compared to Menlow Platform
- **Small size for smartphone form factor**

**Moorestown Performance Technology**

- **Intel Hyper Thread Technology**
- **Intel Burst Performance Technology**

**Intel Hyper-Threading Technology**

Intel Hyper-Threading technology provides excellent Performance/Power efficiency

**Intel Burst Performance Technology**

- Taking advantage of Thermal headroom on Tj and Tdkin for short duration
- On Tj and Tdkin violations, System throttles to recovery points until thermal headroom is available to burst
- Optimizes consumed energy
  - Energy(Wt+E) = Power x time
  - Race to idle
  - Saves energy if
    - Tj/Tdkin < 1/f2
- Update BIOS with recommended profiles for Burst Mode

- Burst mode provides on-demand performance without impacting thermal design
Moorestown Power Reduction

- Active Power Management – Power and Clock Gating
- Use Low Power and Handheld IO
  - LPDDR
- Accelerators (GFX, video decoder)
  - Enable functionality at low power (e.g., HD video)

Active Power Management

- Enables long standby battery life needed for smartphones
  - Through low idle power
- Lower active scenario power by shutting things off that are not used in that mode
  - Switching off video decode block in web browsing

Power Gating

Lincroft SoC: Full ON vs. Power Gated

Aggressive Distributed Power Gating enables up to 50% reduction in idle power

Software Development for Moorestown: Moblin

Opportunity for Customers to Differentiate

Moblin-based Software Stack

Future SoC

- Programmable Accelerator

Current SoC

- IP blocks based on fixed function implementation are not programmable
  - Each data plane block cannot be used for other purpose
- Long Time-to-market (TTM)
  - The block is not programmable
- High Non-Recruent Engineering (NRE) cost
**A Solution for Future SoC**

- Low Power Programmable accelerator
- The challenge is to meet performance requirement under a given power and cost budget

**Our Programmable Accelerator: BSA**

**Programmable Accelerator**

- Different applications can be mapped into the same programmable accelerator
- TTM & NRE cost are reduced

**BSA for H264 Encoding**

**BSA for H264 Decoding**

**Take-away Messages**

- SoC is everywhere!
- The SoC design challenge is to meet exponentially increasing performance requirement under tight power budget and design cost
Q & A

References

• Rapid Repair Website: IPhone 3GS disassembly
• R. Patel, Moorestown Platform: Based on Lincroft SoC Designed for Next Generation Smartphones, HotChips 2009
• Shreekant Thakkar, Moorestown: Intel’s Next Generation Platform for MIDs and Smartphones, IDF 2009
• Steve Leibson, How to Avoid the Traps and Pitfalls of SoC Design, Microprocessor Report, 2009
• Moblin: http://moblin.org