Overview of Today’s Microprocessors and Future Trends

- Computing Evolution
- Technology Scaling
- Microprocessor Families
- Microarchitecture Overview
- Future Challenges
- Some Research Projects of Intel Labs

Initial Developments
- 1946: ENIAC by J.P. Eckert and J. Mauchly
- 1945: Stored program by J.V. Neuman
- 1949: EDSAC by M. Wilkes
- 1952: UNIVAC I and IBM 701

Computing Evolution

The beginning (ENIAC I - 1946)
- Thousands Ops/sec
- Tens of data

Mainframes and Supercomputers (CDC 7600 - 1965)
- Millions Ops/sec
- Millions of data

Mega-scale Computing (IBM PC - 1980)
- Billions Ops/sec
- Billions of data

Giga-scale Computing (Mobile - 2000’s)
- Billions of Ops/sec
- Billions of data

Changing the World
**At the Heart of This Evolution: The Microprocessor**

- **Ultra Low Power** (Intel Atom)
  - Around 50 million transistors
  - Billions of ops/sec

- **High Performance** (Intel Core i7)
  - Around 1 billion transistors
  - HUNDREDS of billions ops/sec

- **The Microprocessor** (Intel 4004 - 1971)
  - 2300 transistors
  - Tens of thousands ops/sec

**Gordon Moore’s Law**

- The number of transistors in a chip doubles every 2 years
- Based on 4 points (year/transistor count) (1959, 1), (1962, 8), (1964, 32), (1965, 64)
- Established on April 19, 1965 in the Electronics Magazine, predicting 65,000 transistors in 1975
- Revised in 1975 in IEEE International Electron Device Meeting

**Technology Scaling Theory**

- X & Y Dimensions scale down by 30%
- Doubles transistor density
- Z-Oxide thickness scales down
- Faster transistor, higher performance
- Vcc & Vt scaling
- Lower active power

**Technology Scaling Trends**

**Today’s Computers**
**Microprocessor Families**
- Pipelined / non-pipelined processors
- In-order / out-of-order processors
- Scalar / superscalar processor
- Vector processors
- Multithreaded processors

**Microprocessor Segments**
- Servers
- Desktop
- Mobile
- Embedded

**Processor Uarch Overview**
- In-order
- In-order or Out-of-Order
- In-order

**Intel Labs Barcelona**
**Mission**
Research on novel processor microarchitectures based on the synergy between software and hardware

**Current Focus**
1. Energy-efficient processors
2. Reliable and adaptable architectures
3. Memory architectures for emerging technologies

**The Present of Computing:**
A Compute Continuum Always Connected

**Intel Labs**
**Intel’s Central Research Organization**
- Nearly 1000 researchers
- Twelve locations globally
- Innovative research models

**The Present of Computing:**
A Compute Continuum Always Connected
The Future: Context-Aware Computing

Platforms that provide timely understanding of the world and real-time responses

Tera-Scale Processors

- Special Purpose Engines
- Integrated IO devices
- Scalable On-die Interconnect Fabric
- Last Level Cache
- Last Level Cache
- Last Level Cache
- Integrated Memory Controllers
- Off Die Interconnect
- High Bandwidth Memory
- Socket Inter-Connect

Tera-Scale Memory

- 80 tile processor with Cu bumps
- Cooler than C4 pitch
- Freya™ C4 pitch
- Memory bandwidth to match the compute power

Tera-Scale IO

- Filter
- Laser
- Modulator
- CMOS Circuitry
- Passive Alignment
- Photodetector
- Silicon Photonics

Tera-Scale Programming

- Languages & programming abstractions
  - Transactional Memory
  - Data parallel operations
  - Lightweight tasks
  - Fine-grain synchronization
- Compilers
  - Multi-language support
  - Dynamic compilation
  - Speculative multithreading

We Can’t Do it Alone

Collaborative R&D Model

Intel Labs

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Core Research

Technology Transfer